CLAIMS

We claim:

1. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming a dielectric layer over the exposed conductive layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

2. The method of claim 1, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as SiOCH; the anti-reflective coating layer is comprised of SiON or SiOC; and the protective film portion is comprised of the elements C, H and O such as C_xH_y.

3. The method of claim 1, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised of the elements Si, O, C and/or H; the anti-reflective coating layer is comprised of SiON; and the protective film portion is comprised of C_2H_4 or C_2H_6.

4. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

5. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

6. The method of claim 1, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

7. The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

8. The method of claim 1, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

9. The method of claim 1, wherein the via opening process is a dry etch process employing an F-based plasma.

10. The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and

plasma power: preferably from about 0 to 3000 W.

11. The method of claim 1, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;

pressure: preferably from about 5 to 250 mTorr;

time: preferably from about 20 to 300 seconds; and

plasma power: preferably from about 50 to 2500 W.

12. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer.

13. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

14. The method of claim 1, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to 1000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

15. The method of claim 1, wherein the protective film portion is also formed over the etched anti-reflective coating layer.

16. The method of claim 1, wherein a via plug is formed within the initial via before formation of the trench opening.

17. The method of claim 1, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

18. The method of claim 1, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

19. The method of claim 1, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

20. The method of claim 1, wherein the protective film portion is comprised of an organic CVD film.

21. The method of claim 1, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100μm.

22. The method of claim 1, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å to 100μm.

23. A method of forming a dual damascene opening, comprising the steps of:

providing a silicon structure having an overlying exposed conductive layer formed thereover; the conductive layer being comprised of copper, aluminum, gold or silver;

forming a dielectric layer over the exposed conductive layer; the dielectric layer being comprised of the elements Si, O, C and/or H such as SiOCH;

forming an anti-reflective coating layer over the dielectric layer; the anti-reflective coating layer being comprised of SiON or SiOC;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer; the protective film portion being comprised of the elements C, H and O such as C_2H_4 or C_2H_6;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

24. The method of claim 23, wherein the conductive layer is comprised of copper; and the anti-reflective coating layer is comprised of SiON.

25. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

26. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

27. The method of claim 23, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

28. The method of claim 23, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

29. The method of claim 23, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; and the protective film portion has a thickness of from about 200 to 1500Å.

30. The method of claim 23, wherein the via opening process is a dry etch process employing an F-based plasma.

31. The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 200°C;

pressure: preferably from about 5 to 300 mTorr;

time: preferably from about 10 to 500 seconds; and

plasma power: preferably from about 0 to 3000 W.

32. The method of claim 23, wherein the via opening process is conducted under the following conditions:

temperature: from about 0 to 100°C;

pressure: preferably from about 5 to 250 mTorr;

time: preferably from about 20 to 300 seconds; and

plasma power: preferably from about 50 to 2500 W.

33. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer.

34. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 50 to 2000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

35. The method of claim 23, including the step of forming an etch stop/liner layer over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 100 to 1000Å and being comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC.

36. The method of claim 23, wherein the protective film portion is also formed over the etched anti-reflective coating layer.

37. The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening.

38. The method of claim 23, wherein a via plug is formed within the initial via before formation of the trench opening; the via plug being comprised of the elements C, H and/or O.

39. The method of claim 23, wherein the formation of trench opening utilizes a patterned masking layer as a mask.

40. The method of claim 23, wherein the formation of trench opening utilizes a patterned photoresist masking layer as a mask.

41. The method of claim 23, wherein the initial via has a width of from about 200 to 3500Å and the trench opening has a width of from about 5000Å to 100μm.

42. The method of claim 23, wherein the initial via has a width of from about 800 to 2500Å and the trench opening has a width of from about 5000Å to 100μm.

43. A method of forming a dual damascene opening, comprising the steps of:

providing a structure having an overlying exposed conductive layer formed thereover;

forming an etch stop/liner layer over the exposed conductive layer;

forming a dielectric layer over the etch stop/liner layer;

forming an anti-reflective coating layer over the dielectric layer;

etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the etch stop/liner layer;

removing the exposed portion of the etch stop/liner layer using a liner removal process to expose a portion of the underlying conductive layer;

forming a protective film portion over at least the exposed portion of the conductive layer;

patterning the anti-reflective coating layer and the dielectric layer to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening.

44. The method of claim 43, wherein the structure includes a silicon substrate or a germanium substrate; the conductive layer is comprised of copper, aluminum, gold or silver; the dielectric layer is comprised of the elements Si, O, C and/or H such as

SiOCH; the anti-reflective coating layer is comprised of SiON or SiOC; the etch stop/liner layer is comprised of the elements Si, O, N and/or C such as Si_3N_4, SiOCN, SiOC or SiC; and the protective film portion is comprised of the elements C, H and O.

45. The method of claim 43, wherein the structure includes a silicon substrate; the conductive layer is comprised of copper; the dielectric layer is comprised SiOCH; the anti-reflective coating layer is comprised of SiON; the etch stop/liner layer is comprised of Si_3N_4, SiOCN, SiOC or SiC; and the protective film portion is comprised of C_2H_4 or C_2H_6.

46. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

47. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

48. The method of claim 43, wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

49. The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 15,000Å; the dielectric layer has a thickness of from about 2000 to 20,000Å; the anti-reflective coating layer has a thickness of from about 50 to 2000Å;

the etch stop/liner liner has a thickness of from about 50 to 2000Å; and the protective film portion has a thickness of from about 50 to 2000Å.

50. The method of claim 43, wherein the conductive layer has a thickness of from about 3000 to 8000Å; the dielectric layer has a thickness of from about 2000 to 15,000Å; the anti-reflective coating layer has a thickness of from about 100 to 1500Å; the etch stop/liner liner has a thickness of from about 100 to 1000Å; and the protective film portion has a thickness of from about 200 to 1500Å.